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Design and Control of an Integrated BMS/DC-DC System for Electric Vehicles

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Sustainable Electrified Transportation Center
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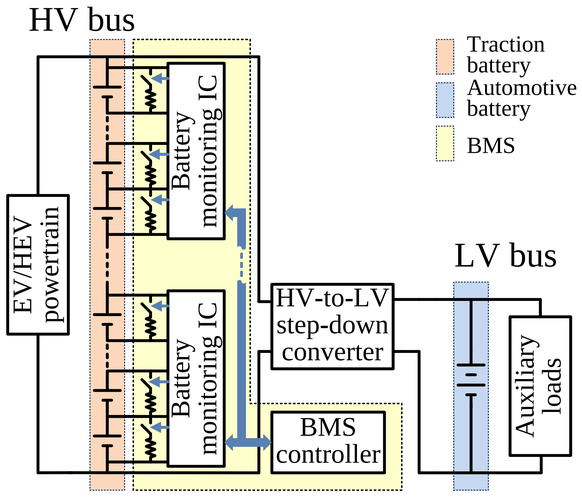
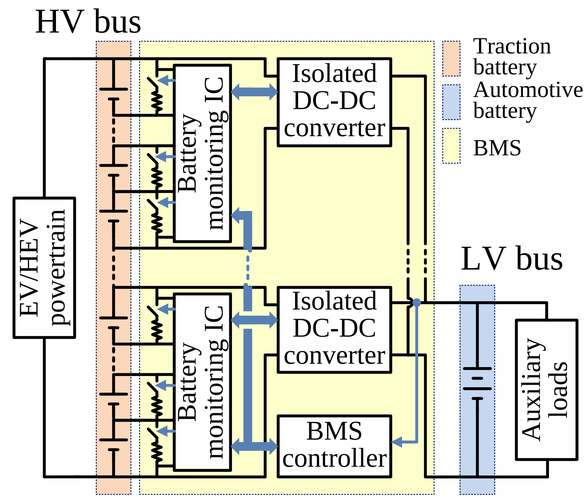
Introduction



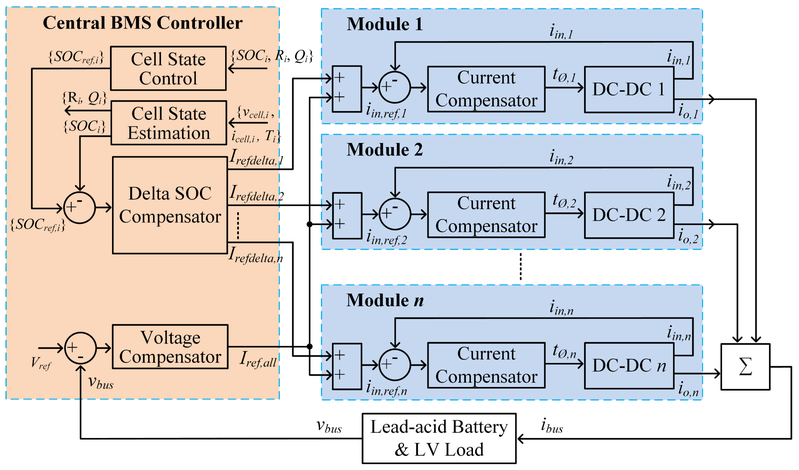
Conventional BMS with passive balancing

- In existing EVs, the battery balancing system and HV-to-LV DC-DC converter operate independently.
- The proposed integrated BMS/DC-DC system can provide enhanced power capability and improved system efficiency by using the LV DC bus load to actively balance battery cells.
- The proposed control strategy uses a combination of central and local controllers to reliably balance the combined requirements for cell state regulation, cell current protection, and bus voltage regulation.



Proposed integrated BMS/DC-DC system

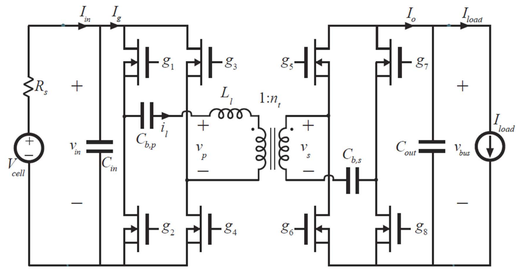
System Control Approach



Proposed control approach for the integrated BMS-DC/DC architecture for electric vehicle applications

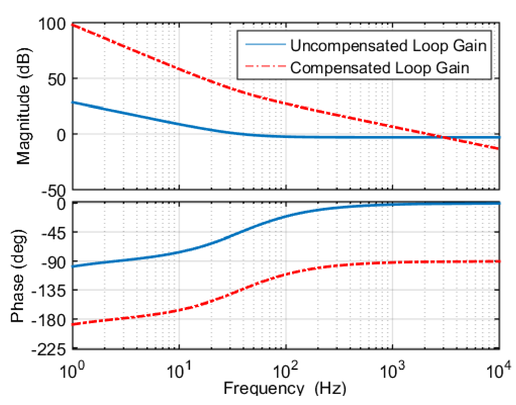
- Each DC-DC module, shown by the dotted blue boxes, has a local current feedback loop.
- The central BMS controller, shown by the dotted orange box, incorporates the voltage compensator and delta SOC compensator that perform LV bus voltage v_{bus} regulation and cell balancing, respectively.

Converter Current Regulation



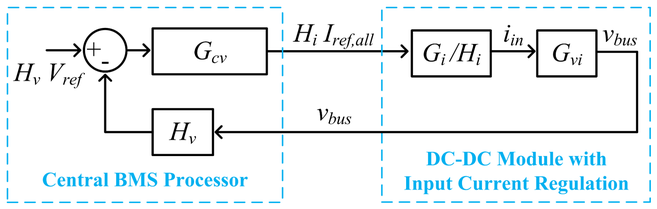
Isolated dual-active-bridge (DAB) converter

- In this work, the isolated DAB converter with phase-shift modulation control is used.
- The current regulation is designed at high speed ($f_{sample} = 10$ kHz) .



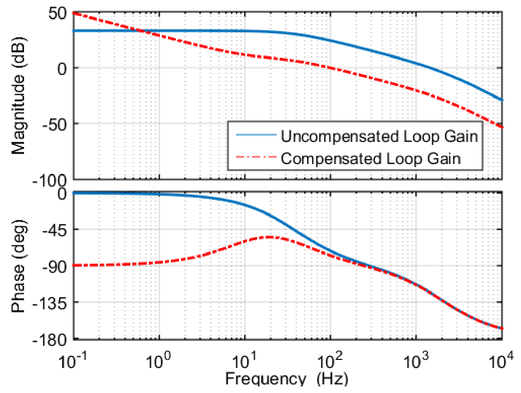
Bode plot of the inner current loop

Bus Voltage Regulation



G_{cv}: PI compensator for voltage loop
G_{vi}: i_{in} to v_{bus} transfer function
G_i: i_{in} close loop transfer function
H_i: current sensor gain
H_v: voltage sensor gain

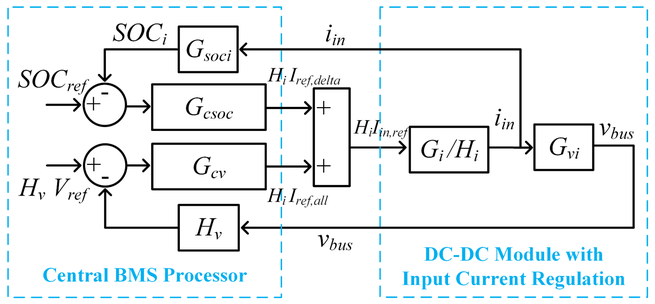
Diagram of the outer voltage loop



Bode plot of the outer voltage loop

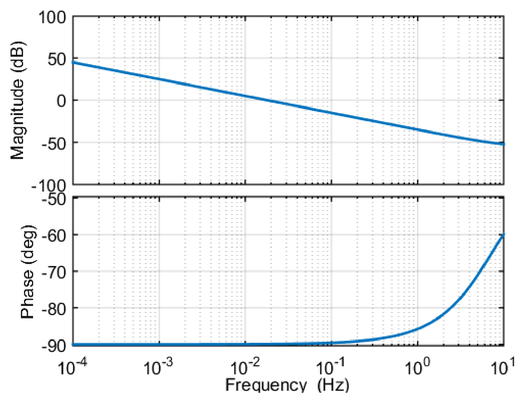
- The DC-DC modules are seen as a virtual DC-DC module in the design.
- The bus voltage regulation is designed at relatively high speed ($f_{sample} = 1$ kHz) .

SOC Regulation Design



G_{csoc}: PI compensator for SOC loop
$G_{soc,i}$: i_{in} to SOC transfer function for cell i

Diagram of the outer SOC loop



Bode plot of the outer SOC loop

- SOC regulation for each cell is running in parallel with bus voltage regulation.
- The SOC regulation for each cell is designed at relatively low speed ($f_{sample} = 1$ Hz) .

Team

Lead Institution

Utah State University, PI: Dr. Regan Zane

Team Institutions

University of Colorado Boulder, PI: Dr. Dragan Maksimovic
University of Colorado Colorado Springs, PI: Dr. Scott Trimboli
National Renewable Energy Laboratory, PI: Dr. Kandler Smith
Ford Motor Company, PI: Dyche Anderson

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References

1. M. Evzelman, M. M. U. Rehman, K. Hathaway, R. Zane, D. Costinett, and D. Maksimović, “Active balancing system for electric vehicles with incorporated low voltage bus,” IEEE Trans. on Power Electronics, vol. 99, pp. 1-1, 2016.
2. M. M. U. Rehman, F. Zhang, R. Zane, and D. Maksimović, “Design and Control of an Integrated BMS/DC-DC System for Electric Vehicles,” COMPEL, 2016.